SDI Audio IP Cores User Guide

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UG-SDI-AUD
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101 Innovation Drive
San Jose, CA 95134
www.altera.com

Contents

SDI Audio IP Overview.....1-1

SDI Audio IP Getting Started.....2-1

Installing and Licensing IP Cores.....2-1

OpenCore Plus IP Evaluation.....2-1

IP Catalog and Parameter Editor.....2-2

Specifying IP Core Parameters and Options.....2-3

Simulating Altera IP Cores in other EDA Tools.....2-4

SDI Audio IP Functional Description.....3-1

SDI Audio Embed IP Core.....3-1

SDI Audio Embed Parameters.....3-2

SDI Audio Extract IP Core.....3-4

SDI Audio Extract Parameters.....3-5

SDI Clocked Audio Input IP Core.....3-6

SDI Audio Clocked Audio Input Parameters.....3-6

SDI Clocked Audio Output IP Core.....3-7

SDI Audio Clocked Audio Output Parameters.....3-7

AES Format.....3-7

Avalon-ST Audio Interface.....3-8

Instantiating the SDI Audio IP Cores.....3-10

Simulating the Testbench.....3-10

Guidelines.....3-11

SDI Audio IP Interface Signals.....4-1

SDI Audio Embed Signals.....4-1

SDI Audio Extract Signals.....4-5

SDI Audio Clocked Input Signals.....4-8

SDI Audio Clocked Output Signals.....4-9

SDI Audio IP Register Interface Signals.....4-10

SDI Audio IP Registers.....5-1

SDI Audio Embed Registers....5-1
SDI Audio Extract Registers....5-4
SDI Clocked Audio Input Registers....5-8
SDI Clocked Audio Output Registers....5-9

SDI Audio IP Design Example....6-1
Components of Design Example....6-1
SDI Transmitter P0....6-2
SDI Duplex....6-2
Audio Extract....6-2
AES Input Module....6-2
AES Output Module....6-2
Audio Embed P0/P1....6-2
Video Pattern Generator P0/P1....6-2
Audio Pattern Generator....6-2
Ancillary Data Insertion P0/P1....6-2
Transceiver Dynamic Reconfiguration Control Logic....6-3
Hardware and Software Requirements....6-3
Running the Design Example....6-4
Transmit SD-SDI with Embedding of Audio Group 1....6-5
Transmit HD-SDI with Embedding of Audio Group 1 and 2....6-5
Transmit 3G-SDI Level A with Embedding of Audio Group 1, 2 and 3....6-6
Transmit 3G-SDI Level B with Embedding of Audio Group 1, 2, 3 and 4....6-6

Additional Information....7-1
Document Revision History....7-1
How to Contact Altera....7-1

SDI Audio IP Overview

1

2014.06.30

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The Altera® SDI Audio MegaCore® functions ease the development of video and image processing designs. For some instances, you combine the audio and video into one digital signal, and at other times you process the audio and video signals separately.

The SDI Audio IP cores are part of the MegaCore IP Library, which is distributed with the Quartus® II software and downloadable from the Altera website at **www.altera.com**.

You can use the following cores to embed, extract or convert audio:

- Audio Embed IP core
- Audio Extract IP core
- Clocked Audio Input IP core
- Clocked Audio Output IP core

You can instantiate the SDI Audio IP cores with the SDI and SDI II IP cores, and configure each Audio IP core at run time using an Avalon-MM slave interface.

Table 1-1: Brief Information About the SDI Audio IP Cores

Item		Description
Release Information	Version	14.0
	Release Date	June 2014
	Ordering Code	IP-SDI
	Product ID(s)	00E6
	Vendor ID	6AF7
IP Core Information	Device Family	Arria® II GX, Arria V, Cyclone® IV GX, Cyclone V, and Stratix® IV GX, and Stratix V FPGA device families. Refer to the **What's New in Altera IP** page of the Altera website for detailed information.

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Related Information

- **Serial Digital Interface (SDI) IP Core User Guide**
  For information about SDI IP core.
- **SDI II IP Core User Guide**
  For information about SDI II IP core.

SDI Audio IP Getting Started 2

2014.06.30

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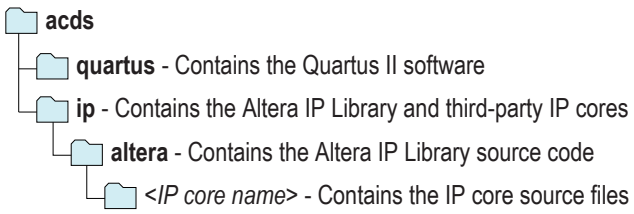
Installing and Licensing IP Cores

The Quartus II software includes the Altera IP Library. The library provides many useful IP core functions for production use without additional license. You can fully evaluate any licensed Altera IP core in simulation and in hardware until you are satisfied with its functionality and performance. Some Altera IP cores, such as MegaCore® functions, require that you purchase a separate license for production use. After you purchase a license, visit the Self Service Licensing Center to obtain a license number for any Altera product.

Figure 2-1: IP Core Installation Path


acds
quartus - Contains the Quartus II software
ip - Contains the Altera IP Library and third-party IP cores
altera - Contains the Altera IP Library source code
<IP core name> - Contains the IP core source files

Note: The default IP installation directory on Windows is **<*drive*>:\altera**<*version number*>; on Linux it is <*home directory*>**/altera/** <*version number*>.

Related Information

- **Altera Licensing Site**
- **Altera Software Installation and Licensing Manual**

OpenCore Plus IP Evaluation

Altera's free OpenCore Plus feature allows you to evaluate licensed MegaCore IP cores in simulation and hardware before purchase. You need only purchase a license for MegaCore IP cores if you decide to take your design to production. OpenCore Plus supports the following evaluations:

- Simulate the behavior of a licensed IP core in your system.
- Verify the functionality, size, and speed of the IP core quickly and easily.
- Generate time-limited device programming files for designs that include IP cores.

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- Program a device with your IP core and verify your design in hardware

OpenCore Plus evaluation supports the following two operation modes:

- Untethered—run the design containing the licensed IP for a limited time.
- Tethered—run the design containing the licensed IP for a longer time or indefinitely. This requires a connection between your board and the host computer.

Note: All IP cores using OpenCore Plus in a design time out simultaneously when any IP core times out.

IP Catalog and Parameter Editor

The Quartus II IP Catalog (**Tools** > **IP Catalog**) and parameter editor help you easily customize and integrate IP cores into your project. You can use the IP Catalog and parameter editor to select, customize, and generate files representing your custom IP variation.

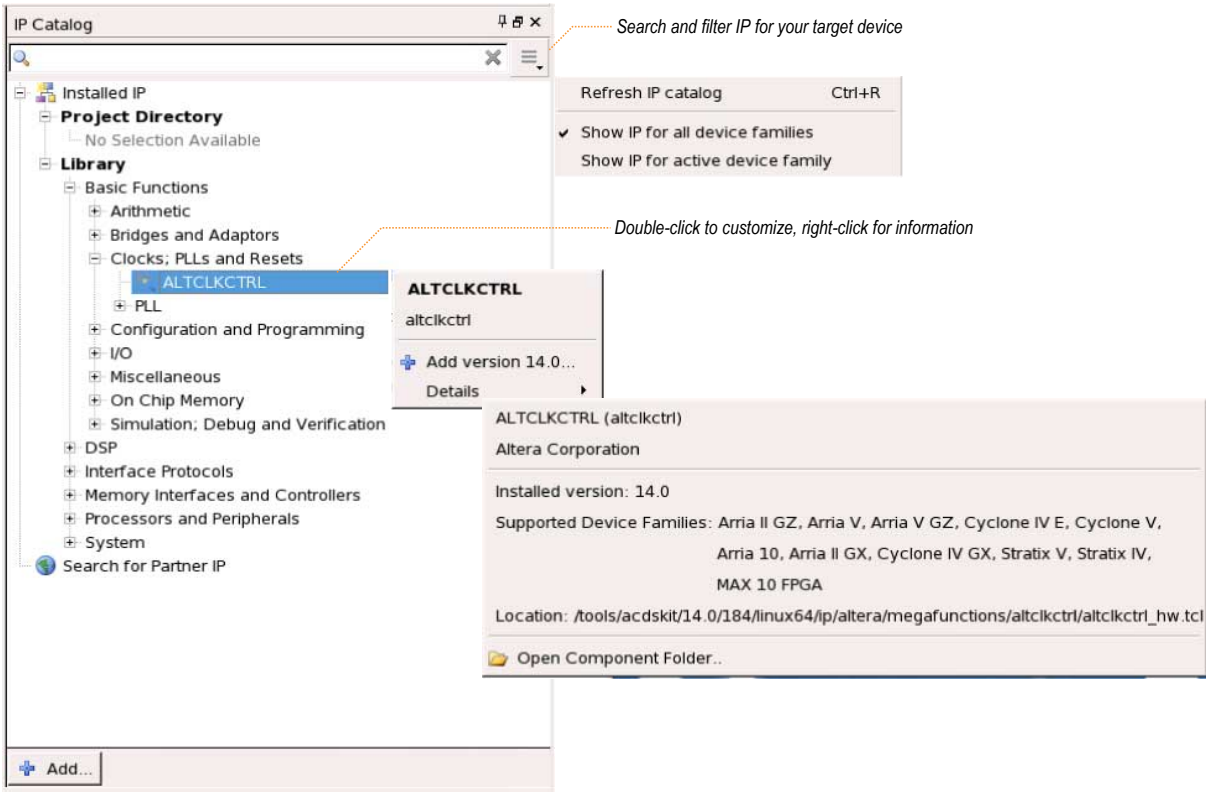
The IP Catalog automatically displays the IP cores available for your target device. Double-click any IP core name to launch the parameter editor and generate files representing your IP variation. The parameter editor prompts you to specify your IP variation name, optional ports, architecture features, and output file generation options. The parameter editor generates a top-level **.qsys** or **.qip** file representing the IP core in your project. Alternatively, you can define an IP variation without an open Quartus II project. When no project is open, select the **Device Family** directly in IP Catalog to filter IP cores by device.

Note: The IP Catalog is also available in Qsys (**View** > **IP Catalog**). The Qsys IP Catalog includes exclusive system interconnect, video and image processing, and other system-level IP that are not available in the Quartus II IP Catalog.

Use the following features to help you quickly locate and select an IP core:

- Filter IP Catalog to **Show IP for active device family** or **Show IP for all device families**.
- Search to locate any full or partial IP core name in IP Catalog. Click **Search for Partner IP**, to access partner IP information on the Altera website.
- Right-click an IP core name in IP Catalog to display details about supported devices, installation location, and links to documentation.

Figure 2-2: Quartus II IP Catalog



Note: The IP Catalog and parameter editor replace the MegaWizard™ Plug-In Manager in the Quartus II software. The Quartus II software may generate messages that refer to the MegaWizard Plug-In Manager. Substitute "IP Catalog and parameter editor" for "MegaWizard Plug-In Manager" in these messages.

Specifying IP Core Parameters and Options

Follow these steps to specify IP core parameters and options.

1. In the IP Catalog (**Tools** > **IP Catalog**), locate and double-click the name of the IP core to customize. The parameter editor appears.
2. Specify a top-level name for your custom IP variation. This name identifies the IP core variation files in your project. If prompted, also specify the target Altera device family and output file HDL preference. Click **OK**.
3. Specify parameters and options for your IP variation:
   - Optionally select preset parameter values. Presets specify all initial parameter values for specific applications (where provided).
   - Specify parameters defining the IP core functionality, port configurations, and device-specific features.
   - Specify options for generation of a timing netlist, simulation model, testbench, or example design (where applicable).

- Specify options for processing the IP core files in other EDA tools.

4. Click **Finish** or **Generate** to generate synthesis and other optional files matching your IP variation specifications. The parameter editor generates the top-level **.qip** or **.qsys** IP variation file and HDL files for synthesis and simulation. Some IP cores also simultaneously generate a testbench or example design for hardware testing.
5. To generate a simulation testbench, click **Generate** > **Generate Testbench System**. **Generate Testbench System** is not available for some IP cores that do not provide a simulation testbench.
6. To generate a top-level HDL example for hardware verification, click **Generate** > **HDL Example**. **Generate** > **HDL Example** is not available for some IP cores.

The top-level IP variation is added to the current Quartus II project. Click **Project** > **Add/Remove Files in Project** to manually add a **.qip** or **.qsys** file to a project. Make appropriate pin assignments to connect ports.

Simulating Altera IP Cores in other EDA Tools

The Quartus II software supports RTL- and gate-level design simulation of Altera IP cores in supported EDA simulators. Simulation involves setting up your simulator working environment, compiling simulation model libraries, and running your simulation.

You can use the functional simulation model and the testbench or example design generated with your IP core for simulation. The functional simulation model and testbench files are generated in a project subdirectory. This directory may also include scripts to compile and run the testbench. For a complete list of models or libraries required to simulate your IP core, refer to the scripts generated with the testbench. You can use the Quartus II NativeLink feature to automatically generate simulation files and scripts. NativeLink launches your preferred simulator from within the Quartus II software.

Figure 2-3: Simulation in Quartus II Design Flow

Note: Altera IP supports a variety of simulation models, including simulation-specific IP functional simulation models and encrypted RTL models, and plain text RTL models. These are all cycle-accurate models. The models support fast functional simulation of your IP core instance using industry-standard VHDL or Verilog HDL simulators. For some cores, only the plain text RTL model is generated, and you can simulate that model. Use the simulation models only for simulation and not for synthesis or any other purposes. Using these models for synthesis creates a nonfunctional design.

Related Information

Simulating Altera Designs

SDI Audio IP Functional Description 3

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The following sections describe the block diagrams and components for the SDI Audio IP cores.

- Audio Embed IP core
- Audio Extract IP core
- Clocked Audio Input IP core
- Clocked Audio Output IP core

SDI Audio Embed IP Core

The SDI Audio Embed Audio IP core embeds audio into the SD-, HD-, and 3G-SDI video standards.

The format of the embedded audio is in accordance with the following standards:

- SMPTE272M-ABCD standard for SD-SDI
- SMPTE299M standard for HD-SDI
- SMPTE299M standard for 3G-SDI (provisional)

This IP core supports AES audio format for 48-kHz sampling rate

This figure shows a block diagram of the SDI Audio Embed IP core.

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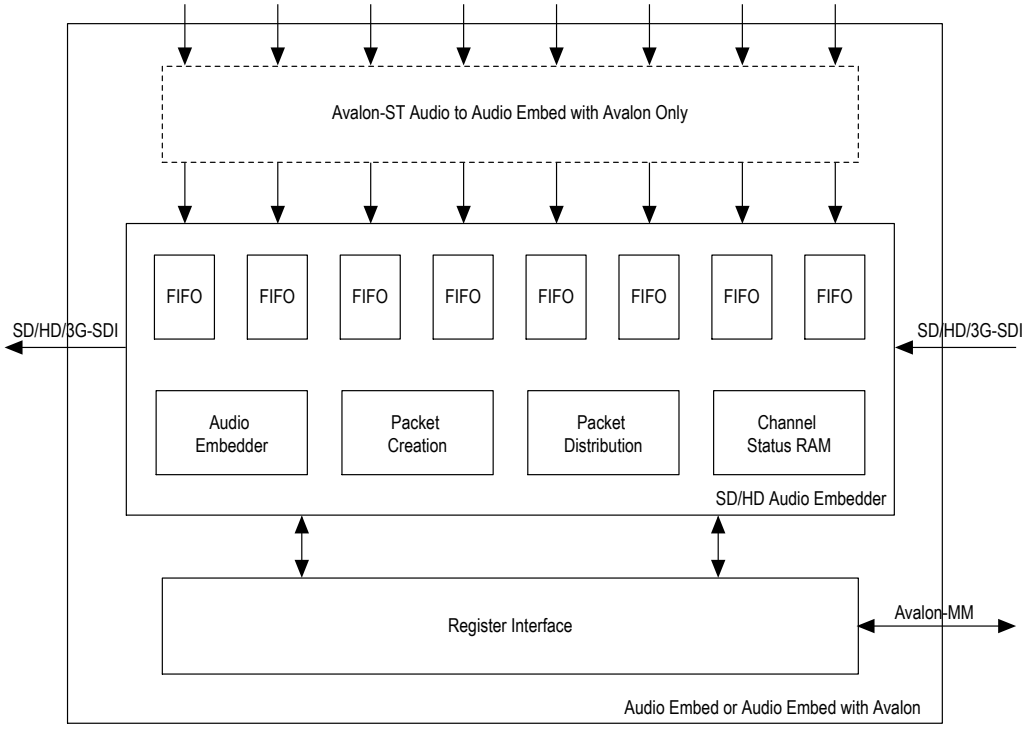
Figure 3-1: SDI Audio Embed IP Core Block Diagram



The SDI Audio Embed IP core embeds up to 16 channels or 8 channel pairs. The input audio can be any of the sample rates permitted by the SMPTE272M-ABCD and SMPTE299M standards; synchronous to the video. If you want to embed audio pairs together in a sample audio group, the audio pairs must be synchronous with each other.

The SDI Audio Embed IP core consists of the following components:

- An encrypted audio embedder core
- A register interface block that provides support for an Avalon-MM control bus

The audio embedder accepts the audio in AES format, and stores each channel pair in an input FIFO buffer. As the embedder places the audio sample in the FIFO buffer, it also records and stores the video clock phase information.

When accepting the audio in AES format, the SDI Audio Embed IP core does one of the following operations:

- maintains the channel-status details
- replaces the channel-status details with the default or the RAM versions

SDI Audio Embed Parameters

The following table lists the parameters for the SDI Audio Embed IP core.

Table 3-1: SDI Audio Embed Parameters

Parameter	Value	Description
Number of supported audio groups	1, 2, 3, 4	Specifies the maximum number of audio groups supported. Each audio group consists of 4 audio channels (2 channel pairs) . You must specify all the four channels to the same sample frequencies.
Async Audio Interface	On or Off	Turn on to enable the Asynchronous input. In this mode, the audio clock provides higher than 64* sample rate.
Frequency of fix_clk	0, 24.576, 25, 50, 100, 200	Sets the expected frequency of the `fix_clk` input; used as frequency reference when detecting the difference between video rate of 1/1.000 or 1/1.001. Setting this parameter to 0 drives `fix_clk` low.
Include SD-SDI 24-bit support	On or Off	Enables the embedding of SD-SDI Extended Data Packets (EDP) for each audio group.
Cleanly remove existing audio	0,1, 2	Enables the removal of existing embedded audio data. When set to 1, the system requires extra storage to delay the video and remove any existing audio from SD-SDI, HD-SDI, or 3G-SDI Level A standard. When set to 2, the system includes extra storage to remove the existing audio from 3G-SDI Level B standard. Select 0 to turn off this parameter.
Channel status RAM	0,1, 2	Enables storage of the custom channel status data. Select 1 to generate a single channel status RAM, or 2 to generate separate RAMs for each input audio pair. Select 0 to turn off this parameter.
Frequency sine wave generator	On or Off	Turn on to enable a four-frequency sine wave generator. You can use the four-frequency sine wave generator as a test source for the audio embedder.
Include clock	On or Off	Turn on to enable a 48-kHz pulse generator synchronous to the video clock. You can use the 48-kHz pulse generator to request data from a sample rate convertor. When you turn on the **Frequency Sine Wave Generator** parameter, the core automatically includes this pulse generator.
Include Avalon-ST interface	On or Off	Turn on to include the SDI Clocked Audio Output IP core. When you turn on this parameter, the Avalon-ST interface signals appear at the top level. Otherwise, the audio input signals appear at the top level.

Parameter	Value	Description
Include Avalon-MM control interface	On or Off	Turn on to include the Avalon-MM control interface. When you turn on this parameter, the register interface signals appear at the top level. Otherwise, the direct control interface signals appear at the top level.

Related Information

SDI Audio Embed Signals on page 4-1

SDI Audio Extract IP Core

The SDI Audio Extract IP core accepts the SD-, HD-, and 3G-SDI from the SDI IP cores and extracts one channel pair of embedded audio.

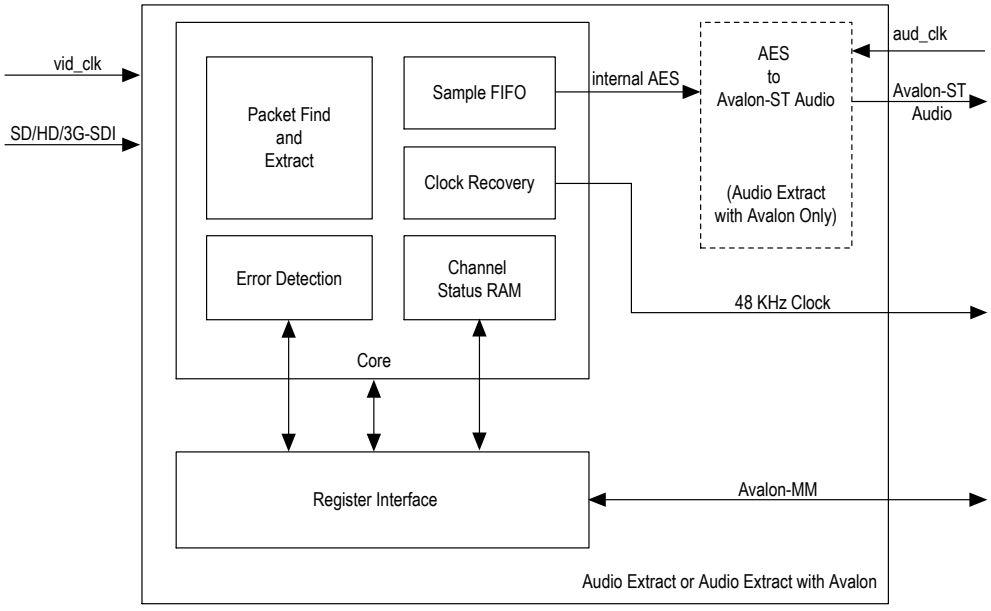
The format of the embedded audio is in accordance with the following standards:

- SMPTE272M-ABCD standard for SD-SDI
- SMPTE299M standard for HD-SDI
- SMPTE299M standard for 3G-SDI (provisional)

If you are extracting more than one channel pair, you must use multiple instances of the component. This IP core supports AES audio format for 48-kHz sampling rate.

This figure shows a block diagram of the SDI Audio Extract IP core.

Figure 3-2: SDI Audio Extract IP Core Block Diagram



The SDI Audio Extract IP core consists of the following components:

- An audio extraction core

- A register interface block that provides support for an Avalon-MM control bus

The clock recovery block recreates a 64 × sample rate clock, which you can use to clock the audio output logic. As the component recreates this clock from a 200-MHz reference clock, the created clock may have a higher jitter than is desirable.

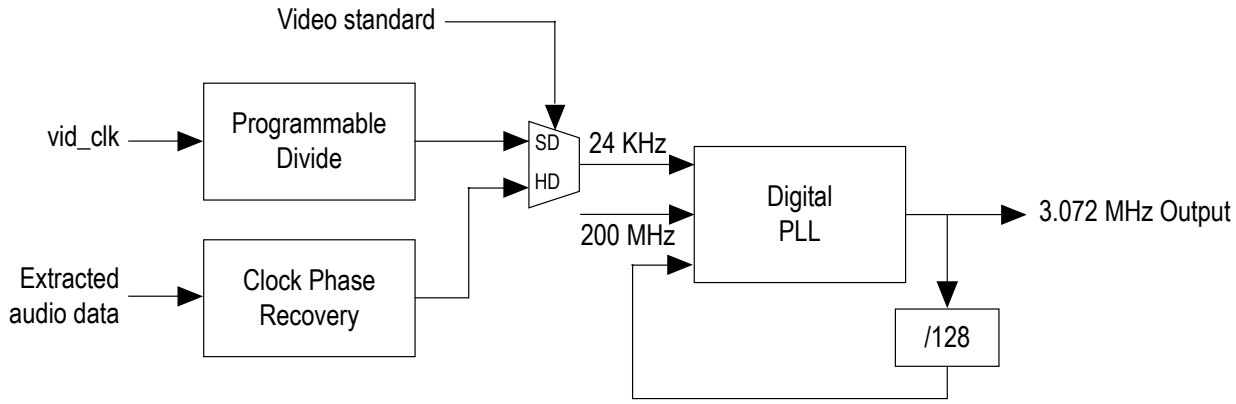
A digital PLL synchronizes this created clock to a 24-kHz reference source.

For the HD-SDI embedded audio, the 24-kHz reference source is the embedded clock phase information.

For the SD-SDI embedded audio, where the embedded clock phase data is not present, you can create the 24-kHz reference signal directly from the video clock.

This figure shows the clock recovery block diagram.

Figure 3-3: Clock Recovery Block Diagram



SDI Audio Extract Parameters

The following table lists the parameters for the SDI Audio Extract IP core.

Table 3-2: SDI Audio Extract Parameters

Parameter	Value	Description
Include SD-SDI 24-bit support	On or Off	Enables the extra logic to recover the EDP ancillary packets from SD-SDI inputs.
Channel status RAM	On or Off	Turn on to store the received channel status data.
Include error checking	On or Off	Turn on to enable extra error-checking logic to use the error status register.
Include status register	On or Off	Turn on to enable extra logic to report the audio FIFO status on the `fifo_status` port or register.

Parameter	Value	Description
Include clock	On or Off	Turn on to enable the logic to recover both a sample rate clock and a 64 × sample rate clock. With HD-SDI inputs, the core generates the output by using the embedded clock phase information. With SD-SDI inputs, the core generates this output by using the counters running on the 27-MHz video clock. This generation limits the SD-SDI embedded audio to being synchronous to the video.
Include Avalon-ST interface	On or Off	Turn on to include the SDI Clocked Audio Input IP core. When you turn on this parameter, the Avalon-ST interface signals appear at the top level. Otherwise, the audio input signals appear at the top level.
Include Avalon-MM control interface	On or Off	Turn on to include the Avalon-MM control interface. When you turn on this parameter, the register interface signals appear at the top level. Otherwise, the direct control interface signals appear at the top level.

Related Information

SDI Audio Extract Signals on page 4-5

SDI Clocked Audio Input IP Core

The Clocked Audio Input IP core converts clocked audio in AES formats to Avalon-ST audio.

For a typical AES input, for each channel, the clocked audio input function does the following operations:

- Creates a 192-bit validity word, user word and channel status word
- Presents the words as a control packet after the audio data packet

SDI Audio Clocked Audio Input Parameters

The following table lists the parameters for the SDI Clocked Audio Input IP cores.

Table 3-3: SDI Clocked Audio Input Parameters

Parameter	Value	Description
FIFO size	3–10	Defines the internal FIFO depth. For example, a value of 3 means $2^3 = 8$.
Include Avalon-MM control interface	On or Off	Turn on to include the Avalon-MM control interface. When you turn on this parameter, the register interface signals appear at the top level. Otherwise, the direct control interface signals appear at the top level.

SDI Clocked Audio Output IP Core

The SDI Clocked Audio Output IP core accepts clocked Avalon-ST audio and converts to audio in modified AES formats.

SDI Audio Clocked Audio Output Parameters

The following table lists the parameters for the SDI Clocked Audio Output IP cores.

Table 3-4: SDI Clocked Audio Output Parameters

Parameter	Value	Description
FIFO size	3–10	Defines the internal FIFO depth. For example, a value of 3 means $2^3 = 8$.
Include Avalon-MM control interface	On or Off	Turn on to include the Avalon-MM control interface. When you turn on this parameter, the register interface signals appear at the top level. Otherwise, the direct control interface signals appear at the top level.

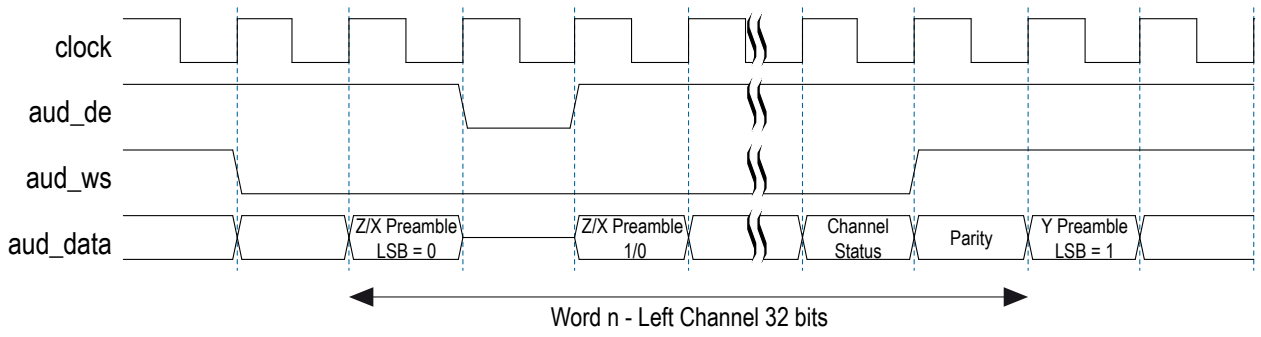
AES Format

The SDI cores use the AES standard. The Audio Engineering Society (AES), together with the European Broadcasting Union (EBU), created a digital audio transmission standard known as the AES/EBU standard. The AES standard is a digital audio standard for transporting digital audio signals serially between devices.

Using the AES format requires the entire 64-bit AES frame to be sent serially. As the AES defines the preambles as biphase mark codes, which cannot be directly decoded to 4 bits, you must replace the preambles with X = 0000b, Y = 0001b, and Z = 0010b. This internal AES format serializes the bit-parallel data words by sending the least significant bits (LSB) first, with the audio sample (up to 24 bits).

This figure shows the timing diagram of the internal AES format.

Figure 3-4: Internal AES Format Timing Diagram

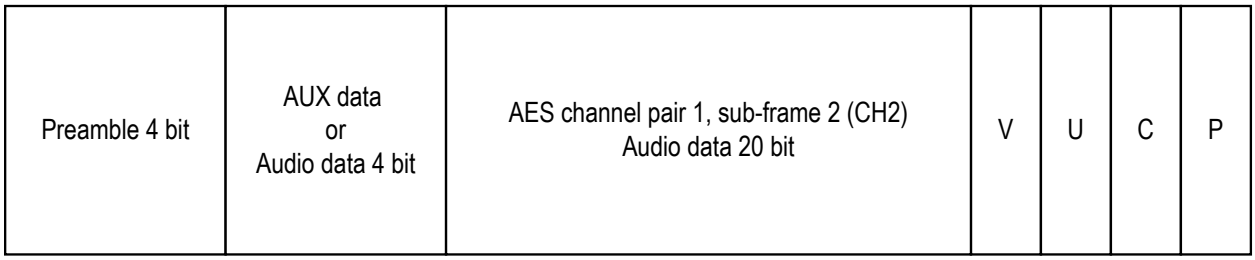


Avalon-ST Audio Interface

To allow the standard components inside Qsys to interconnect, you must define the Avalon-ST audio interface. The Avalon-ST audio interface must carry audio to and from physical AES3 interfaces; which means to support the AES3 outputs, the interface must transport the extra V, U, and C bits. You may create the P bit.

Each audio block consists of 192 frames, and each frame has channels 1 and 2. Each frame has a combination of the bits shown in the following figure.

Figure 3-5: AES Format

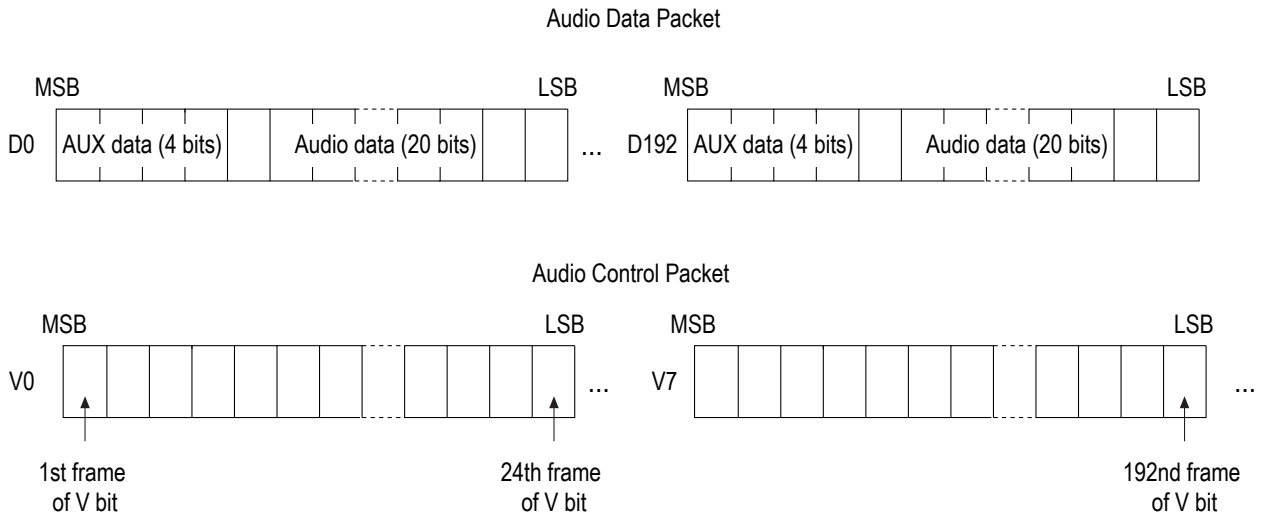


The Avalon-ST is a packet-based interface, which carries audio information as a sequence of data packets. The functions define the types of packets as audio data packets and audio control packets.

This figure shows the audio data and audio control packets for Avalon-ST audio interface.

Figure 3-6: Audio Data and Audio Control Packets for Avalon-ST Audio Interface

The sequence of audio control packets begins with V bit, U bit, and finally C bit. The audio control packets for U and C bits are similar to V bits.



The Avalon-ST audio protocol separates the audio data from the control or status data to facilitate audio data processing. The protocol defines that the data is packed LSB first, which matches the AES3 data. The

audio data size is configurable at compile time and matches the audio data sample size. Including the aux, the audio data word would be 24 bits.

In Avalon-ST audio, the data is packed as 24 bit symbols, typically with 1 symbol per beat [23:0]. The core transmits the audio control data as a packet after the audio data to meet the latency requirements.

The packet type identifier defines the packet type. The packet type identifier is the first value of any packet, when the start of packet signal is high. The audio data packet identifier is 0×A and the audio control data packet identifier is 0×E.

The table below lists the packet types.

Table 3-5: Avalon-ST Packet Types

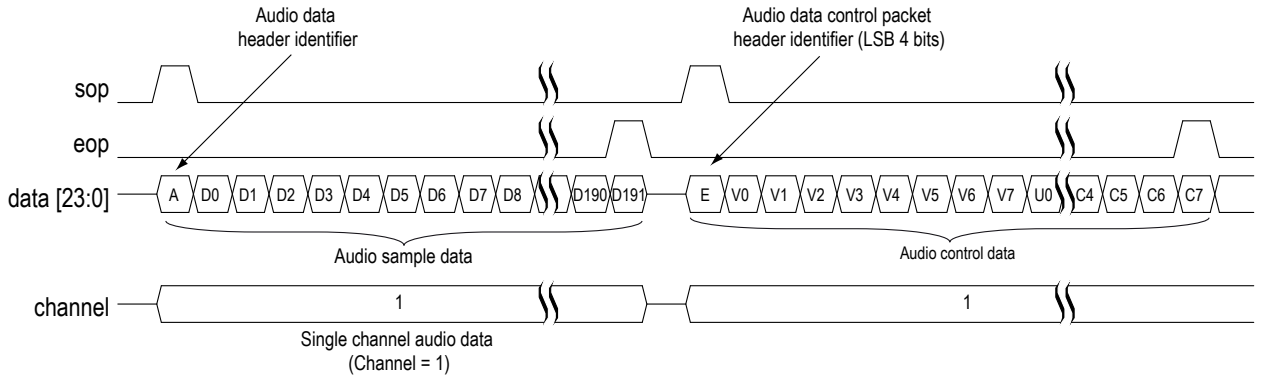
Type Identifier	Description
0	Video data packet
1–8	User packet types
10	Audio data packet
14	Audio control data packet
15	Video control data packet
9–15	Reserved

The preamble data, XYZ from AES, describes whether the data is at the start of a block and which channel the audio refers to. In Avalon-ST audio protocol, you are not required to transport the preamble data because the information stored in the data is described by the start of packet, end of packet, and channel signals.

The start of packet, end of packet, and channel signals indicate the start of the audio sample data and the associated audio channel.

For a single audio channel, the channel signal indicates channel 1 for all valid samples. This figure shows an example of a single audio channel.

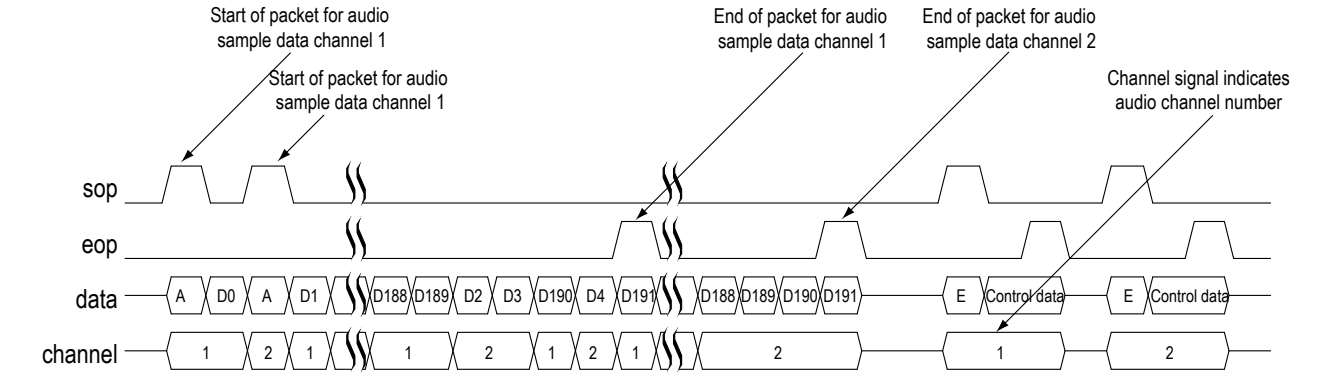
Figure 3-7: Single Audio Channel



For multiple channels, the Avalon-ST interface standard allows the packets to interleave across the channels. By interleaving, the interface allows multiple audio sources to be multiplexed and demultiplexed.

This figure shows an example of two audio channels, where the channel signal indicates either channel 1 or channel 2. Each channel has a start of packet and an end of packet signal, which allows the channel interleaving and de-interleaving.

Figure 3-8: Multiple Audio Channels



Instantiating the SDI Audio IP Cores

You can instantiate the SDI Audio Embed and Audio Extract IP cores in the following ways:

- Instantiate within Qsys with the audio inputs exposed outside Qsys.
- Instantiate within Qsys with the audio inputs exposed as Avalon-ST Audio within Qsy.
  As the SDI Audio Embed and Extract IP cores use an Avalon-MM slave interface to access the control registers, the most convenient way for you to instantiate the components are within Qsys. You are provided with the component declaration TCL files to support either the ordinary AES audio inputs or the Avalon-ST audio interface.
- Instantiate directly in RTL with a CPU register interface.
  You can instantiate the SDI Audio Embed and Audio Extract IP cores directly in your RTL and drive the direct control interface signals directly without the accompanying Avalon-MM register interface
- Instantiate the encrypted core directly on RTL with control ports.

Simulating the Testbench

Altera provides a fixed testbench as an example to simulate the SDI Audio cores. Use this testbench to simulate the SDI Audio Embed and the associated SDI Audio Extract IP cores, and the SDI Clocked Audio Input and the associated SDI Clocked Audio Output IP cores.

You can obtain the testbench from **ip/altera/audio_ip/simulation** directory.

To use the testbench with the ModelSim simulator, follow these steps:

1. Open the Quartus II software.
2. On the File menu, click the **New Project Wizard**.
3. Specify the working directory to **ip/altera/audio_ip/simulation/megacore_build**, and give a sensible name for your project and top-level entity.
4. Click **Next**, and select **Stratix IV** for the device family.

5. Click **Finish**.
6. In the IP Catalog (**Tools > IP Catalog**), locate and double-click the **variant audio_embed_avalon_top.v** file.
   The SDI Audio Embed parameter editor appears.
7. In the SDI Audio Embed parameter editor, click **Finish** to regenerate the **variant audio_embed_avalon_top.v** file and produce the simulation model.
8. Repeat steps 6 to 9 for the remaining variant files in the **megacore_build** directory.
9. In a text editor, open the simulation script, **simulation/run.tcl**. Edit the script to point to your installation of the Quartus II software.
   For example, `set quartusdir /tools/acds/14.0/157/linux32/quartus/eda/sim_lib/`
10. Start the ModelSim simulator.
11. Run **run.tcl** in the simulation directory. This file compiles the design.
    A selection of signals appears on the waveform viewer. The simulation runs automatically, providing a pass or fail indication upon completion.

Guidelines

When you use the testbench to simulate the IP cores, consider the following guidelines:

- Select the video standard for the video test source through the generic `G_TEST_STD` of the testbench entity. Set 0, 1, 2 or 3 to select SD-SDI, HD-SDI, 3G-SDI Level A, or 3G-SDI Level B.
- The audio test source uses the 48-kHz clock output from the SDI Audio Embed IP core. The audio test sample comprises an increasing count which allows the testbench to check the extracted audio at the far end of the processing chain.
- The SDI Audio Embed IP core accepts these video and audio test sources to create a video stream with embedded audio. The SDI Audio Extract IP core then receives the resulting stream to recover the embedded audio. Examine this audio sequence to ensure that the count pattern that was created is preserved.
- The synchronisation requirements of the receive FIFO buffer in the SDI Audio Extract IP core allows you to repeat the occasional sample from the SDI Audio Extract IP core. Synchronisation may take up to a field period of typically 16.7 ms to complete.
- Select `G_INCLUDE_AVALON_ST = 1`, if you want to instantiate another SDI Audio Embed IP core with Avalon-ST interface (with embedded clocked audio output component) and the associated SDI Audio Extract IP core with Avalon-ST interface (with embedded clocked audio input component) in this testbench.

SDI Audio IP Interface Signals

4

2014.06.30

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SDI Audio Embed Signals

The following tables list the signals for the SDI Audio Embed IP cores.

This table lists the general input and output signals.

Table 4-1: SDI Audio Embed General Input and Output Signals

Signal	Width	Direction	Description
`reset`	[0:0]	Input	This signal resets the system.
`fix_clk`	[0:0]	Input	This signal provides the frequency reference used when detecting the difference between video standards using 1 and 1/1.001 clock rates. If its frequency is 0, the signal only detects either one of the clock rates. The core limits the possible frequencies for this signal to 24.576 MHz, 25 MHz, 50 MHz, 100 MHz, and 200 MHz. Set the required frequency using the **Frequency of fix_clk** parameter.
`vid_std_rate`	[0:0]	Input	If you set the **Frequency of fix_clk** parameter to 0, you must drive this signal high to detect a video frame rate of 1/1.001 and low to detect a video frame rate of 1. For other settings of the **Frequency of fix_clk** parameter, the core automatically detects these frame rates and drives this signal low.
`vid_clk48`	[0:0]	Output	The 48 kHz output clock that is synchronous to the video. This clock signal is only available when you turn on the **Frequency Sine Wave Generator** or **Include Clock** parameter.

This table lists the video input and output signals.

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Table 4-2: SDI Audio Embed Video Input and Output Signals

Signal	Width	Direction	Description
vid_clk	[0:0]	Input	The video clock that is typically 27 MHz for SD-SDI, 74.25 MHz or 74.17 MHz for HD-SDI, or 148.5 MHz or 148.35 MHz for 3G-SDI standards. You can use higher clock rates with the vid_datavalid signal. Set exclusive clock group to aud_clk and vid_clk to prevent unstable or flickering image.
vid_std	[1:0]	Input	Indicates the received video standard. Applicable for 3G-SDI, dual standard, and triple standard modes only. Set this signal to indicate the following formats: • [00] for10-bit SD-SDI • [01] for 20-bit HD-SDI • [10] for 3G-SDI Level B • [11] for 3G-SDI Level A
vid_datavalid	[0:0]	Input	Assert this signal when the video data is valid.
vid_data	[19:0]	Input	Receiver protocol reset signal. This signal must be driven by the rx_rst_proto_out reset signal from the transceiver block. This signal carries luma and chroma information. SD-SDI: • [19:10] Unused • [9:0] Cb,Y, Cr, Y multiplex HD-SDI and 3G-SDI Level A: • [19:10] Y • [9:0] C 3G-SDI Level B: • [19:10] Cb,Y, Cr, Y multiplex (link A) • [9:0] Cb,Y, Cr, Y multiplex (link B)
vid_out_datavalid	[0:0]	Output	The core drives this signal high during valid output video clock cycles.
vid_out_trs	[0:0]	Output	The core drives this signal high during the first 3FF clock cycle of a video timing reference signal; the first two 3FF cycles for 3G-SDI Level B. This signal provides easy connection to the SDI IP cores.
vid_out_ln	[10:0]	Output	The video line signal that provides for easy connection to the SDI IP cores. To observe the correct video out line number, allow two-frame duration for the audio embed IP to correctly embed and show the line number.
vid_out_data	[19:0]	Output	The video output signal.

This table lists the audio input signals.

Table 4-3: SDI Audio Embed Audio Input Signals

N is the number of audio group.

Signal	Width	Direction	Description
aud_clk	[2N–1:0]	Input	Set this clock to 3.072 MHz that is synchronous to the extracted audio. In asynchronous mode, set this to any frequency above 3.072 MHz. Altera recommends that you set this clock to 50 MHz. For SD-SDI inputs, this mode of operation limits the core to embedding audio that is synchronous to the video. For HD-SDI inputs, this clock must either be generated from the optional 48 Hz output or the audio must be synchronous to the video. Set exclusive clock group to aud_clk and vid_clk to prevent unstable or flickering image.
aud_de	[2N–1:0]	Input	Assert this data enable signal to indicate valid information on the aud_ws and aud_data signals. In synchronous mode, the core ignores this signal.
aud_ws	[2N–1:0]	Input	Assert this word select signal to provide framing for deserialization and to indicate left or right sample of channel pair.
aud_data	[2N–1:0]	Input	Internal AES data signal from the AES input module.

This table lists the Avalon-ST audio signals when you instantiate the SDI Audio Embed IP core in Qsys.

Table 4-4: SDI Audio Embed Avalon-ST Audio Signals

n is the number of audio channels, the value starts from from 0 to n-1.

Signal	Width	Direction	Description
aud(n)_clk	[0:0]	Input	Clocked audio clock. All the audio input signals are synchronous to this clock.
aud(n)_ready	[0:0]	Output	Avalon-ST ready signal. Assert this signal when the device is able to receive data.
aud(n)_valid	[0:0]	Input	Avalon-ST valid signal. The core asserts this signal when it receives data.
aud(n)_sop	[0:0]	Input	Avalon-ST start of packet signal. The core asserts this signal when it is starting a new frame.
aud(n)_eop	[0:0]	Input	Avalon-ST end of packet signal. The core asserts this signal when it is ending a frame.
aud(n)_channel	[7:0]	Input	Avalon-ST select signal. Use this signal to select a specific channel.
aud(n)_data	[23:0]	Input	Avalon-ST data bus. This bus transfers data.

This table lists the register interface signals. The register interface is a standard 8-bit wide Avalon-MM slave.

Table 4-5: SDI Audio Embed Register Interface Signals

Signal	Width	Direction	Description
reg_clk	[0:0]	Input	Clock for the Avalon-MM register interface.
reg_reset	[0:0]	Input	Reset for the Avalon-MM register interface.
reg_base_addr	[5:0]	Input	Reset for the Avalon-MM register interface.
reg_burst_count	[5:0]	Input	Transfer size in bytes.
reg_waitrequest	[0:0]	Output	Wait request.
reg_write	[7:0]	Input	Write request.
reg_writedata	[0:0]	Input	Data to be written to target.
reg_read	[0:0]	Input	Read request.
reg_readdatavalid	[0:0]	Output	Requested read data valid after read latency.
reg_readdata	[7:0]	Output	Data read from target.

This table lists the direct control interface signals. These signals are exposed as ports if you turn off the **Include Avalon-MM Control Interface** parameter.

Table 4-6: SDI Audio Embed Direct Control Interface Signals

Signal	Width	Direction	Description
reg_clk	[0:0]	Input	Clock for the direct control interface.
audio_control	[7:0]	Input	Assert this 8-bit signal to enable the audio channels. Each bit controls one audio channel.
extended_control	[7:0]	Input	This signal does the same function as the extended control register.
video_status	[7:0]	Output	This signal does the same function as the video status register.
sd_edp_control	[7:0]	Output	This signal does the same function as the SD EDP control register.
audio_status	[7:0]	Output	This signal does the same function as the audio status register.
cs_control	[15:0]	Input	This signal does the same function as the channel status control register.
strip_control	[7:0]	Input	This signal does the same function as the strip control register.
strip_status	[7:0]	Output	This signal does the same function as the strip status register.
sine_freq_ch1	[7:0]	Input	This signal does the same function as the sine channel 1 frequency register.
sine_freq_ch2	[7:0]	Input	This signal does the same function as the sine channel 2 frequency register.
sine_freq_ch3	[7:0]	Input	This signal does the same function as the sine channel 3 frequency register.

Signal	Width	Direction	Description
sine_freq_ch4	[7:0]	Input	This signal does the same function as the sine channel 4 frequency register.
csram_addr	[5:0]	Input	Channel status RAM address.
csram_we	[0:0]	Input	Drive this signal high for a single cycle of reg_clk signal to load the value of the csram_data port into the channel status RAM at the address on the csram_addr port. If each input audio pair gets separate channel status RAMs, this signal addresses the RAM selected by the extended_control port.
csram_data	[7:0]	Input	Channel status data. This signal does the same function as the channel status RAM register in Table 4–9.

Related Information

- **SDI Audio Embed Registers** on page 5-1
- **SDI Audio IP Register Interface Signals** on page 4-10

All SDI Audio IP cores use the same register interface signals.

SDI Audio Extract Signals

The following tables list the signals for the SDI Audio Extract IP core.

This table lists the clock recovery input and output signals.

Table 4-7: SDI Audio Extract Recovery Input and Output Signals

Signal	Width	Direction	Description
reset	[0:0]	Input	This signal resets the system.
fix_clk	[0:0]	Input	Assert this 200 MHz reference clock when you turn on the **Include Clock** parameter. If you do not turn on the **Include Clock** parameter, tie this signal low.
aud_clk_out	[0:0]	Output	The core asserts this 64 × sample rate clock (3.072 MHz audio clock) when you turn on the **Include Clock** parameter. You use this clock to clock the audio interface in synchronous mode. As the core creates this clock digitally, it is prone to higher levels of jitter.
aud_clk48_out	[0:0]	Output	The core asserts this sample rate clock when you turn on the **Include Clock** parameter.

This table lists the video input signals.

Table 4-8: SDI Audio Extract Video Input Signals

Signal	Width	Direction	Description
vid_clk	[0:0]	Input	The video clock that is typically 27 MHz for SD-SDI, 74.25 MHz or 74.17 MHz for HD-SDI, or 148.5 MHz or 148.35 MHz for 3G-SDI standards. You can use higher clock rates with the vid_datavalid signal.
vid_std	[1:0]	Input	Indicates the received video standard. Applicable for 3G-SDI, dual standard, and triple standard modes only. Set this signal to indicate the following formats: • 00b for10-bit SD-SDI • 01b for 20-bit HD-SDI • 11b for 3G-SDI Level B • 10b for 3G-SDI Level A
vid_datavalid	[0:0]	Input	Assert this signal when the video data is valid.
vid_data	[19:0]	Input	This signal carries luma and chroma information. SD-SDI: • [19:10] Unused • [9:0] Cb,Y, Cr, Y multiplex HD-SDI and 3G-SDI Level A: • [19:10] Y • [9:0] C 3G-SDI Level B: • [19:10] Cb,Y, Cr, Y multiplex (link A) • [9:0] Cb,Y, Cr, Y multiplex (link B)
vid_locked	[0:0]	Input	Assert this signal when the video is locked.

This table lists the audio input and output signals.

Table 4-9: SDI Audio Extract Audio Input and Output Signals

Signal	Width	Direction	Description
aud_clk	[0:0]	Input	Set this clock to 3.072 MHz that is synchronous to the extracted audio. For SD-SDI inputs, this mode of operation limits the core to extracting audio that is synchronous to the video. For HD-SDI inputs, you must generate this clock from the optional 48 kHz output or the audio must be synchronous to the video.

Signal	Width	Direction	Description
aud_ws_in	[0:0]	Input	Some audio receivers provide a word select output to align the serial outputs of several audio extract cores. In these circumstances, assert this signal to control the output timing of the audio extract externally, otherwise set it to 0. This signal must be a repeating cycle of high for 32 aud_clk cycles followed by low for 32 aud_clk cycles.
aud_de	[0:0]	Output	Assert this data enable signal to indicate valid information on the aud_ws and aud_data signals. In synchronous mode, the core ignores this signal. The core asserts this data enable signal to indicate valid information on the aud_ws and aud_data signals. In synchronous mode, the core drives this signal high.
aud_ws	[0:0]	Output	The core asserts this word select signal to provide framing for deserialization and to indicate left or right sample of channel pair.
aud_data	[0:0]	Output	The core asserts this signal to extract the internal AES audio signal from the AES output module.

This table lists the Avalon-ST audio signals when you instantiate the SDI Audio Extract IP core in Qsys.

Table 4-10: SDI Audio Extract Avalon-ST Audio Signals

n is the number of audio channels, the value starts from from 0 to n-1.

Signal	Width	Direction	Description
aud(n)_clk	[0:0]	Input	Clocked audio clock. All the audio input signals are synchronous to this clock.
aud(n)_ready	[0:0]	Output	Avalon-ST ready signal. Assert this signal when the device is able to receive data.
aud(n)_valid	[0:0]	Input	Avalon-ST valid signal. The core asserts this signal when it receives data.
aud(n)_sop	[0:0]	Input	Avalon-ST start of packet signal. The core asserts this signal when it is starting a new frame.
aud(n)_eop	[0:0]	Input	Avalon-ST end of packet signal. The core asserts this signal when it is ending a frame.
aud(n)_channel	[7:0]	Input	Avalon-ST select signal. Use this signal to select a specific channel.
aud(n)_data	[23:0]	Input	Avalon-ST data bus. This bus transfers data.

This table lists the direct control interface signals. The direct control interface is internal to the SDI Audio Extract IP core.

Table 4-11: SDI Audio Extract Direct Control Interface Signals

Signal	Width	Direction	Description
reg_clk	[0:0]	Input	Clock for the direct control interface.
audio_control	[7:0]	Input	This signal does the same function as the audio control register.
audio_presence	[7:0]	Input	This signal does the same function as the audio presence register.
audio_status	[7:0]	Output	This signal does the same function as the audio status register.
sd_edp_presence	[7:0]	Output	This signal does the same function as the SD EDP presence register.
error_status	[7:0]	Output	This signal does the same function as the error status register.
error_reset	[15:0]	Input	Set any bit of this port high for a single cycle of reg_clk to clear the corresponding bit of the error_status signal. Setting any of bits [3:0] high for a clock cycle resets the entire 4-bit error counter.
fifo_status	[7:0]	Input	This signal does the same function as the FIFO status register.
fifo_reset	[7:0]	Input	Set high for a single cycle of reg_clk to clear the underflow or overflow field of the fifo_status signal.
clock_status	[7:0]	Input	This signal does the same function as the clock status register.
csram_addr	[5:0]	Input	Channel status RAM address. The contents of the selected address will be valid on the csram_data signal after one cycle of reg_clk.
csram_data	[7:0]	Input	Channel status data. This signal does the same function as the channel status RAM.

Related Information

- **SDI Audio Extract Registers** on page 5-4
- **SDI Audio IP Register Interface Signals** on page 4-10

All SDI Audio IP cores use the same register interface signals.

SDI Audio Clocked Input Signals

The following tables list the signals for the SDI Audio Clocked Input IP cores.

This table lists the input and output signals.

Table 4-12: SDI Audio Clocked Input Input and Output Signals

Signal	Width	Direction	Description
aes_clk	[0:0]	Input	Audio input clock.
aes_de	[0:0]	Input	Audio data enable.

Signal	Width	Direction	Description
aes_ws	[0:0]	Input	Audio word select.
aes_data	[0:0]	Input	Audio data input in internal AES format.

This table lists the Avalon-ST audio signals when you instantiate the SDI Audio Clocked Input IP core in Qsys.

Table 4-13: SDI Audio Clocked Input Avalon-ST Audio Signals

Signal	Width	Direction	Description
aud_clk	[0:0]	Input	Clocked audio clock. All the audio input signals are synchronous to this clock.
aud_ready	[0:0]	Input	Avalon-ST ready signal. Assert this signal when the device is able to receive data.
aud_valid	[0:0]	Output	Avalon-ST valid signal. The core asserts this signal when it produces data.
aud_sop	[0:0]	Output	Avalon-ST start of packet signal. The core asserts this signal when it is starting a new frame.
aud_eop	[0:0]	Output	Avalon-ST end of packet signal. The core asserts this signal when it is ending a frame.
aud_data	[23:0]	Output	Avalon-ST data bus. The core asserts this signal to transfer data.

This table lists the direct control interface signals. The direct control interface is internal to the audio extract component.

Table 4-14: SDI Audio Clocked Input Direct Control Interface Signals

Signal	Width	Direction	Description
channel0	[7:0]	Input	Indicates the channel number of audio channel 1.
channel1	[7:0]	Input	Indicates the channel number of audio channel 2.
fifo_status	[7:0]	Input	Drive bit 7 high to reset the clocked audio input FIFO buffer.
fifo_reset	[0:0]	Output	Assert this signal when the clocked audio input FIFO buffer overflows.

Related Information

SDI Audio IP Register Interface Signals on page 4-10
All SDI Audio IP cores use the same register interface signals.

SDI Audio Clocked Output Signals

The following tables list the signals for the SDI Audio Clocked Output IP cores.

This table lists the input and output signals.

Table 4-15: SDI Audio Clocked Output Input and Output Signals

Signal	Width	Direction	Description
aes_clk	[0:0]	Input	Audio input clock.
aes_de	[0:0]	Output	Audio data enable.
aes_ws	[0:0]	Output	Audio word select.
aes_data	[0:0]	Output	Audio data input in internal AES format.

This table lists the Avalon-ST audio signals when you instantiate the SDI Audio Clocked Output IP core in Qsys.

Table 4-16: SDI Audio Clocked Output Avalon-ST Audio Signals

Signal	Width	Direction	Description
aud_clk	[0:0]	Input	Clocked audio clock. All the audio input signals are synchronous to this clock.
aud_ready	[0:0]	Output	Avalon-ST ready signal. Assert this signal when the device is able to receive data.
aud_valid	[0:0]	Input	Avalon-ST valid signal. The core asserts this signal when it receives data.
aud_sop	[0:0]	Input	Avalon-ST start of packet signal. The core asserts this signal when it is starting a new frame.
aud_eop	[0:0]	Input	Avalon-ST end of packet signal. The core asserts this signal when it is ending a frame.
aud_data	[23:0]	Input	Avalon-ST data bus. This bus transfers data.

Related Information

SDI Audio IP Register Interface Signals on page 4-10
All SDI Audio IP cores use the same register interface signals.

SDI Audio IP Register Interface Signals

All SDI Audio IP cores use the same register interface signals.

The register interface is a standard 8-bit wide Avalon-MM slave.

Table 4-17: SDI Audio IP Register Interface Signals

Signal	Width	Direction	Description
reg_clk	[0:0]	Input	Clock for the Avalon-MM register interface.
reg_reset	[0:0]	Input	Reset for the Avalon-MM register interface.

Signal	Width	Direction	Description
reg_base_addr	[5:0]	Input	Reset for the Avalon-MM register interface.
reg_burst_count	[5:0]	Input	Transfer size in bytes.
reg_waitrequest	[0:0]	Output	Wait request.
reg_write	[7:0]	Input	Write request.
reg_writedata	[0:0]	Input	Data to be written to target.
reg_read	[0:0]	Input	Read request.
reg_readdatavalid	[0:0]	Output	Requested read data valid after read latency.
reg_readdata	[7:0]	Output	Data read from target.

SDI Audio IP Registers 5

2014.06.30

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SDI Audio Embed Registers

The following tables list the registers for the SDI Audio Embed IP core.

Table 5-1: SDI Audio Embed Register Map

Bytes Offset	Name
00h	Audio Control Register
01h	Extended Control Register
02h	Video Status Register
03h	SD EDP Control Register
04h	Channel Status Control Registers (3:0)
05h	Channel Status Control Registers (7:4)
06h	Strip Control Register
07h	Strip Status Register
08h	Sine Channel 1 Frequency
09h	Sine Channel 2 Frequency
0Ah	Sine Channel 3 Frequency
0Bh	Sine Channel 4 Frequency
0Ch	Audio Status Register
0Dh-0Fh	Reserved
10h-3Fh	Channel Status RAM (0×00), (0×01), ... (0×2F)

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Table 5-2: SDI Audio Embed Registers

Bit	Name	Access	Description
Audio Control Register			
7:0	Audio group enable	RW	Enables the embedding of each audio group. When working with HD-SDI or 3G-SDI video, this register also enables the embedding of the audio control packet when one or more audio groups are enabled. The following bits correspond to the number of audio groups you specify: • Bit [1:0] = Audio group 1 • Bit [3:2] = Audio group 2 • Bit [5:4] = Audio group 3 • Bit [7:6] = Audio group 4
Extended Control Register			
2:0	Channel status RAM select	RW	When you specify the **Channel Status RAM** parameter to 2, this field selects the channel pair for the RAM written to by registers 10h to 3Fh. If you specify the **Channel Status RAM** parameter to 0 or 1, ignore this signal.
3	Unused	—	Reserved for future use.
4	Test sine generator enable	RW	When set to 1b, this bit ignores the audio inputs and uses the output of the sine generator as the data for each audio group.
6:5	Link AB Control	RW	This register applies only for 3G-SDI Level B standard. Controls which link the ancillary data is embedded in. • 00b = No data is embedded • 01b = Data is embedded only in Link B. • 10b = Data is embedded only in Link A (default value). • 11b = Data is embedded in Link A and Link B at the same time. When set to 11b, the IP core inserts new packets after any existing ancillary data on Link A and in the identical location on Link B. If the packet distribution of existing ancillary data on Link B differs, existing packets may be corrupted. In these circumstances, Altera recommends you use two separate instances of the ancillary embedder.
7	Unused	—	Reserved for future use.

Video Status Register			

7:0	Active channel	RO	Reports the detected video input standard.
			• Bits[7:5] = Picture structure code. Defined values for picture structure code are:
			  • 001b = 486 or 576 line SD-SDI
			  • 100b = 720 line HD-SDI
			  • 101b = 1080 line HD-SDI
			  • 010b = 1080 line 3G-SDI
			  • 011b = 1080 line 3GA-SDI
			  • 110b = 720 line 3GA-SDI
			  • 111b = 720 line 3GB-SDI
			• Bit[4] = 0b—Interlace or segmented frame, 1b—Progressive.
			• Bits[3:0] = Frame rate code. Defined values for frame rate code (in Hz) are:
			  • 0010b = 23.97
			  • 0011b = 24
			  • 0101b = 25
			  • 0110b = 29.97
			  • 0111b = 30
			  • 1001b = 50
			  • 1010b = 59.94
			  • 1011b = 60

SD EDP Control Register			
3:0	Enable SD EDP	RW	Enables the embedding of SD-SDI Extended Data Packets (EDP) for each audio group.
7:4	Enable SD ACP	RW	Enables the embedding of SD-SDI Audio Control Packets (ACP) for each audio group.
Channel Status Control Register			
7:0	CS mode select	RW	When set to 00b, the core keeps the existing channel status data. When set to 01b, the core replaces the channel status data with default values. When set to 10b, the core replaces the data with the contents of the appropriate channel status RAM. The following bits correspond to the number of audio groups you specify: • Bit [1:0] = Audio group 1 • Bit [3:2] = Audio group 2 • Bit [5:4] = Audio group 3 • Bit [7:6] = Audio group 4

Strip Control Register			
3:0	Strip enable	RW	Enables the removal of both ACP and ADP (and any SD-SDI EDP) for each of the four audio groups.
7:4	Unused	—	Reserved for future use.
Strip Status Register			
3:0	Data packet present	RO 3:0	Reports which audio data groups are detected in the SDI stream. When in 3G-SDI Level B mode, this register reports the presence of audio on Link A (Link B should be a duplicate).
7:4	Control packet present	RO	Reports which audio control groups are detected in the SDI stream. When in 3G-SDI Level B mode, this register reports the presence of audio on Link A (Link B should be a duplicate).
Sine Channel *n* Frequency			
7:0	Sine channel frequency	RW	Defines the frequency of the generated audio.
Audio Status Register			
3:0	Audio group presence	RO	Reports which audio groups are detected in the SDI stream.
4	Frame lock	RO	Reports whether the video frame with the embedded audio is locked.
Channel Status RAM			
7:0	Channel status data	WO	Write accesses within the address range 10h to 3Fh to the channel status RAM. This field returns the 24 bytes of channel status for X channels starting at address 10h to 27h, and the 24 bytes of channel status for Y channels starting at address 28h to 3Fh.

Related Information

SDI Audio Embed Signals on page 4-1

SDI Audio Extract Registers

The following tables list the registers for the SDI Audio Extract IP core.

Table 5-3: SDI Audio Extract Register Map

Bytes Offset	Name
00h	Audio Control Register
01h	Audio Presence Register
02h	Audio Status Register
03h	SD EDP Presence Register
04h	Error Status Register
05h	Reserved
06h	FIFO Status Register
07h	Clock Status Register
08h-09h	Reserved
10h-3Fh	Channel Status RAM (0×00), (0×01), ... (0×2F)

Table 5-4: SDI Audio Extract Registers

Bit	Name	Access	Description
Audio Control Register			
0	Enable	RW	Enables the audio extraction component and internal AES output.
3:1	Extract pair	RW	Defines the audio pair that the component extracts. For example: • [000] = Extract the first channel pair of audio signal • [111] = Extract the eighth channel pair of audio signal
4	Extract pair MSB	RW	For 3G-SDI Level A standard, this field extends the extract pair field to allow for future implementations with 32 embedded audio channels. For 3G-SDI Level B standard, this field selects the active video half of the 3G multiplex.
5	Mute	RW	Drive this register high to mute the audio output.
7:6	Unused	—	Reserved for future use.

Audio Presence Register			
3:0	Data packet present	RW	When you specify the **Channel Status RAM** parameter to 2, this field selects the channel pair for the RAM written to by registers 10h to 3Fh. If you specify the **Channel Status RAM** parameter to 0 or 1, ignore this signal. Reports which audio data groups are detected in the SDI stream. The following bits correspond to the number of audio groups detected: • Bit [0] = Audio group 1 • Bit [1] = Audio group 2 • Bit [2] = Audio group 3 • Bit [3] = Audio group 4
7:4	Control packet present	RO	Reports which audio control packets are detected in the SDI stream.
Audio Status Register			

3:0	Active channel	RO	Reports the detected video input standard.
			• Bits[7:5] = Picture structure code. Defined values for picture structure code are:
			  • 001b = 486 or 576 line SD-SDI
			  • 100b = 720 line HD-SDI
			  • 101b = 1080 line HD-SDI
			  • 010b = 1080 line 3G-SDI
			• Bit[4] = 0b—Interlace or segmented frame, 1b—Progressive.
			• Bits[3:0] = Frame rate code. Defined values for frame rate code (in Hz) are:
			  • 0010b = 23.97
			  • 0011b = 24
			  • 0101b = 25
			  • 0110b = 29.97
			  • 0111b = 30
			  • 1001b = 50
			  • 1010b = 59.94
			  • 1011b = 60

4	Asynchronous	RW	Reflects the asx bit of the RATE (sampling rate) field of the audio control packet.
6:5	Sample rate	RW	Reports the X1 and X0 bits of the sample rate code from the RATE field of the audio control packet.
7	Status valid	RW	Set to 1b when the audio control packet is present in the video stream.

SD EDP Presence Register			
3:0	EDP Present	RO	Reports which audio extended data groups are detected in the SD-SDI stream.
7:4	Unused	—	Reserved for future use.
Error Status Register			
3:0	Error counter	RW	Counts up to 15 errors since last reset. Write 1b to any bit of this field to reset the entire counter to zero.
4	Ancillary CS fail	RW	Indicates that an error has been detected in the ancillary packet checksum. This bit stays set until cleared by writing 1b to this register.
5	Ancillary parity fail	RW	Indicates that an error has been detected in at least one of the parity fields: • ancillary packet parity bit • audio sample parity bit (for SD-SDI) • AES sample parity bit (for HD-SDI This bit stays set until cleared by writing 1b to this register.
6	Channel status CRC fail	RW	Indicates that an error has been detected in the channel status CRC. This bit stays set until cleared by writing 1b to this register.
7	Audio packet ECRC fail	RW	Indicates that an error has been detected in the ECRC that forms part of the HD audio data packet. This bit stays set until cleared. To clear, write 1b to this register.
FIFO Status Register			
6:0	FIFO fill level	RO	Reports the amount of data in either the audio output FIFO or the Avalon-ST audio FIFO when the optional Avalon-ST Audio interface is used.
7	Overflow/underflow	RW	This register bit goes high if one of the following occurs (based on the output mode used): • underflow or overflow of the audio output FIFO • overflow of the Avalon-ST audio FIFO This register always goes high at the beginning, so you must clear the audio FIFO first for the register to indicate underflow or overflow.
Clock Status Register			
4:0	Offset	RO	Defines the frequency of the generated audio.
6:5	Unused	—	Reserved for future use.

Clock Status Register			
7	74.17-MHz video clock	RO	To create a 48-kHz signal synchronous to the video clock, you must detect whether a 1 or 1/1.001 video clock rate is used. If you detect a 1/1.001 video clock rate, this field returns high.
Channel Status RAM			
7:0	Channel status data	WO	Read accesses within the address range 10h to 3Fh to the channel status RAM. This field returns the 24 bytes of channel status for X channel starting at address 10h, and the 24 bytes of channel status for Y channel starting at address 28h.

SDI Clocked Audio Input Registers

The following tables list the registers for the SDI Clocked Audio Input IP core.

Table 5-5: SDI Clocked Audio Input Register Map

Bytes Offset	Name
00h	Channel 0 Register
01h	Channel 1 Register
02h	FIFO Status Register
03h	FIFO Reset Register

Table 5-6: SDI Clocked Audio Input Registers

Bit	Name	Access	Description
Channel 0 Register			
7:0	Channel 0	RW	The user-defined channel number of audio channel 0.
Channel 1 Register			
7:0	Channel status RAM select	RW	The user-defined channel number of audio channel 1.
FIFO Status Register			
7:0	Active channel	RO	This sticky bit reports the overflow of the clocked audio input FIFO.
FIFO Reset Register			
6:0	Unused	WO	Reserved for future use.
7	FIFO reset	WO	Resets the clocked audio FIFO.

SDI Clocked Audio Output Registers

The following tables list the registers for the SDI Clocked Audio Output IP core.

Table 5-7: SDI Clocked Audio Output Register Map

Bytes Offset	Name
00h	Channel 0 Register
01h	Channel 1 Register
02h	FIFO Status Register
03h	FIFO Reset Register

Table 5-8: SDI Clocked Audio Output Registers

Bit	Name	Access	Description
Channel 0 Register			
7:0	Channel 0	RW	The user-defined channel number of audio channel 0.
Channel 1 Register			
7:0	Channel status RAM select	RW	The user-defined channel number of audio channel 1.
FIFO Status Register			
7:0	Active channel	RO	This sticky bit reports the overflow of the clocked audio output FIFO.
FIFO Reset Register			
6:0	Unused	WO	Reserved for future use.
7	FIFO reset	WO	Resets the clocked audio FIFO.

SDI Audio IP Design Example

6

2014.06.30

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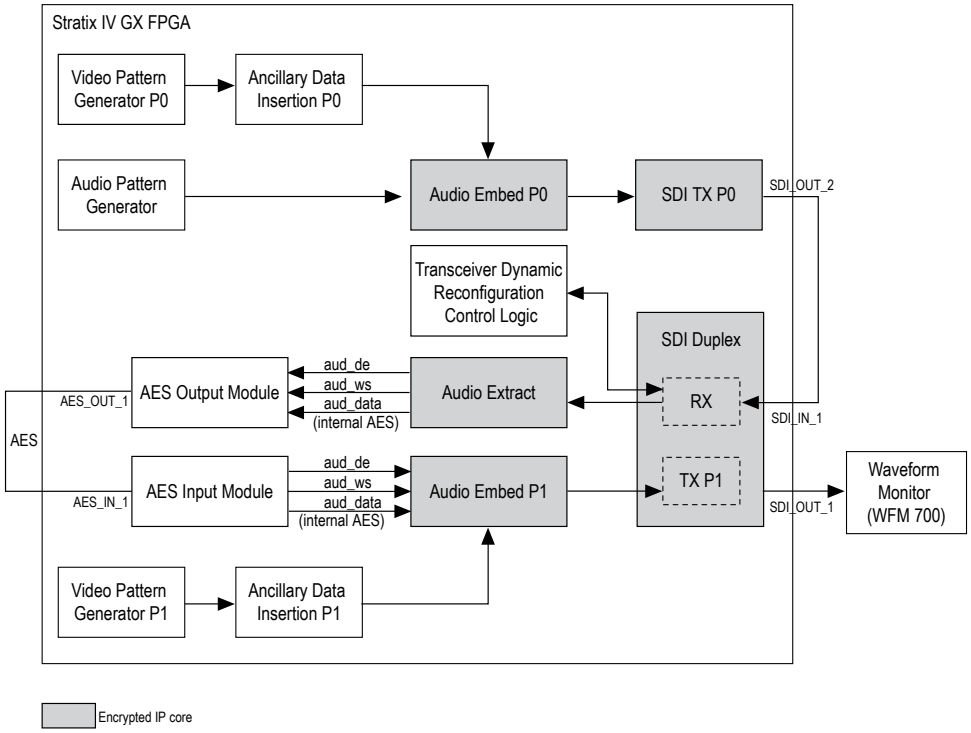
Altera provides a design example with the SDI Audio Embed and Extract IP cores. This design example includes the SDI Audio IP cores and instances of the SDI IP cores.

This section discusses the requirements and related procedures to demonstrate the SDI Audio example design with the Stratix IV GX Audio Video Development Kit.

Components of Design Example

This figure shows a high-level block diagram of the design example.

Figure 6-1: High-Level Block Diagram of Stratix IV GX FPGA



The following sections describe the various elements in design example.

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SDI Transmitter P0

The triple-standard SDI transmitter that outputs a 3G-SDI (2.970 Gbps), HD-SDI (1.485 Mbps), or SD-SDI (270 Mbps) data stream. This transmitter gets the parallel data source from the SDI Audio Embed IP core. The SDI Audio Embed component embeds the internally generated audio in AES format into the internally generated video. The transmitter transmits the serial signal through a BNC cable to the receiver of the SDI duplex instance.

SDI Duplex

The triple-standard SDI duplex provides a full-duplex SD-SDI, HD-SDI, and 3G-SDI standards. The SDI duplex instance routes the received data to the SDI Audio Extract IP core to extract the AES audio. The SDI Audio Embed IP core embeds the internally generated audio in AES format into the internally generated video. The transmitter in this duplex connects its output to the external waveform monitor, such as the WFM700.

Audio Extract

The Audio Extract IP core extracts the embedded AES audio from the SDI stream. The Audio Extract IP core routes the extracted AES audio to the AES output of the daughter card.

AES Input Module

The AES input module converts the AES signal to `aud_de`, `aud_ws`, and `aud_data` (internal AES) signals to interface with Audio Embed P1. When this module interfaces with the Audio Embed IP core, both must use the same clock.

AES Output Module

The AES output module converts the `aud_de`, `aud_ws`, and `aud_data` signals to AES signal. This module configures the extracted internal AES audio signal (`aud_data`) without the biphase mark encoding. When this module interfaces with the Audio Extract IP core, it must use the same clock as the Audio Extract IP core.

Audio Embed P0/P1

The Audio Embed P0 embeds the AES audio generated by the Audio Pattern Generator into the video stream, as a transmitting data, for the SDI transmitter P0. The Audio Embed P1 embeds the AES audio from the external AES input into the video stream for the SDI duplex

Video Pattern Generator P0/P1

You can configure the internal video pattern generator to output an SD-SDI, HD-SDI, 3G-SDI Level A or 3G-SDI Level B colorbar pattern.

Audio Pattern Generator

You can configure the internal audio pattern generator to create an AES audio test sample that comprises an increasing count. You configure the generator using the 48-kHz clock output from the Audio Embed IP core.

Ancillary Data Insertion P0/P1

The Ancillary Data Insertion module inserts the ancillary data defined by SMPTE352 into the SDI video stream.

Transceiver Dynamic Reconfiguration Control Logic

The transceiver dynamic reconfiguration control logic block handles the reconfiguration of the receiver in the SDI duplex.

Hardware and Software Requirements

The design example requires the following hardware and software:

- Stratix IV GX Audio Video Development Kit—Stratix IV GX FPGA development board and SDI HSMC
- SDI IP Core
- SDI Audio Embed IP Core
- SDI Audio Extract IP Core
- The Quartus II software, version 14.0

Hardware Setup

This table lists the function of each LED on the Stratix IV GX FPGA development board.

Table 6-1: Function of Each LED on the Stratix IV GX FPGA Development Board

LED	Description
D23	Indicates the presence of audio group 1 data packet in the incoming embedded audio.
D22	Indicates the presence of audio group 2 data packet in the incoming embedded audio.
D21	Indicates the presence of audio group 3 data packet in the incoming embedded audio.
D20	Indicates the presence of audio group 4 data packet in the incoming embedded audio.
D19	Indicates that the receiver of the SDI duplex IP Core is alignment locked.
D18	Indicates that the receiver of the SDI duplex IP Core is TRS locked.
D17	Indicates that the receiver of the SDI duplex IP Core is frame locked.
D16	Indicates the recovered clock heartbeat of the receiver.
D13	Indicates the ancillary checksum failure.
D12	Indicates the ancillary parity failure.
D11	Indicates the channel status CRC failure.
D10	Indicates the audio packet failure.
D9–D8	Indicate the SDI receive video standards. 00 = SD-SDI, 01 = HD-SDI, 11 = 3G-SDI Level A, 10 = 3G-SDI Level B
D7–D6	Indicate the SDI transmit video standards. 00 = SD-SDI, 01 = HD-SDI, 11 = 3G-SDI Level A, 10 = 3G-SDI Level B

This table lists the function of each user-defined dual in-line package (DIP) switch settings.

Table 6-2: Function of Each DIP Switch

DIP Switch	Description
8	Resets the system.
7	Resets the Audio Extract IP core status registers.
6–3	Unused.
2–1	Configure the internally-generated video standards for both SDI transmitters. 00 = SD-SDI: When 00, enables the embedding of audio group 1, 01 = HD-SDI: When 01, enables the embedding of audio group 1 and 2, 11 = 3G-SDI Level A: When 11, enables the embedding of audio group 1, 2, and 3, 10 = 3G-SDI Level B: When 10, enables the embedding of audio group 1, 2, 3, and 4

Related Information

AN 600: Serial Digital Interface Reference Design for Stratix IV Devices
For information about how the Stratix IV GX FPGA development board connects to the SDI HSMC.

Running the Design Example

To run the design example, you must set up the development board.

To set up the development board, follow these steps:

1. Set up the board connections.
   a. Connect the SDI HSMC to HSMA port on the Stratix IV GX development board.
   b. Connect the development board to the power supply.
   c. Connect the `SDI_OUT_2` port (SDI TX P0) to the `SDI_IN_1` port (SDI duplex) using external BNC cable.
   d. Connect the `AES_OUT_1` port to the `AES_IN_1` port using external BNC cable.
   e. Connect the `SDI_OUT_1` port (SDI duplex) to the external waveform monitor so that you can analyze the embedded audio in the SDI video stream.
2. Launch the Quartus II software.
   a. On the File menu, click **Open Project**, navigate to **ip/altera/audio_ip/example/s4gx_sdi_audio/s4gxsdi_audio.qpf**, and click Open.
   b. On the Processing menu, click **Start Compilation**.
3. Download the Quartus II-generated SRAM Object File (**.sof**).
   After you set up the board, run the different configurations described in the following sections.

Transmit SD-SDI with Embedding of Audio Group 1

To transmit the SD-SDI video standard, follow these steps:

1. Set DIP switch[2:1] = 00
2. The demonstration runs and the LEDs indicate the following conditions:
   a. LED D16 blinks indicating the heartbeat of the receiver's recovered clock.
   b. LED D17 illuminates when the receiver is frame locked.
   c. LED D18 illuminates when the receiver is TRS locked.
   d. LED D19 illuminates when the receiver is alignment locked.
   e. LED D23 illuminates when the data packet of audio group 1 is detected in the incoming SDI stream.

   This figure shows the condition of the LEDs.

Figure 6-2: Condition of LEDs for Transmitting SDI-SDI Video Standard

3. The external waveform monitor (WFM700) displays the following observation:
   a. Colorbar video pattern
   b. Video format detected is 625i 50.00
   c. Embedded audio standard detected is SMPTE272M
   d. Audio channel pairs (1,2) and (3,4) are present

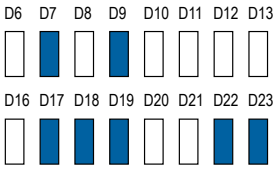
Transmit HD-SDI with Embedding of Audio Group 1 and 2

To transmit the HD-SDI video standard, follow these steps:

1. Set DIP switch[2:1] = 01
2. The demonstration runs and the LEDs indicate the following conditions:
   a. LEDs D6 and D7 indicate the internal video pattern generator signal standard.
   b. LEDs D8 and D9 indicate the receive video standard.
   c. LED D16 blinks indicating the heartbeat of the receiver's recovered clock. The frequency is blinking is slower than the previous demonstration.
   d. LED D17 illuminates when the receiver is frame locked.
   e. LED D18 illuminates when the receiver is TRS locked.
   f. LED D19 illuminates when the receiver is alignment locked.
   g. LEDs D23 and D22 illuminate when the data packet of audio groups 1 and 2 are detected in the incoming SDI stream.

   This figure shows the condition of the LEDs.

Figure 6-3: Condition of LEDs for Transmitting HDI-SDI Video Standard



3. The external waveform monitor (WFM700) displays the following observation:
   a. Colorbar video pattern
   b. Video format detected is 1080i 60.00
   c. Embedded audio standard detected is SMPTE299M
   d. Audio channel pairs (1,2), (3,4), (5,6) and (7,8) are present

Transmit 3G-SDI Level A with Embedding of Audio Group 1, 2 and 3

To transmit the 3G-SDI Level A video standard, follow these steps:

1. Set DIP switch[2:1] = 11
2. The demonstration runs and the LEDs indicate the following conditions:
   a. LEDs D6 and D7 indicate the internal video pattern generator signal standard.
   b. LEDs D8 and D9 indicate the receive video standard.
   c. LED D16 blinks indicating the heartbeat of the receiver's recovered clock..
   d. LED D17 illuminates when the receiver is frame locked.
   e. LED D18 illuminates when the receiver is TRS locked.
   f. LED D19 illuminates when the receiver is alignment locked.
   g. LEDs D23, D22 and D21 illuminate when the data packet of audio groups 1, 2 and 3 are detected in the incoming SDI stream.

   This figure shows the condition of the LEDs.

Figure 6-4: Condition of LEDs for Transmitting 3G-SDI Level A Video Standard

Transmit 3G-SDI Level B with Embedding of Audio Group 1, 2, 3 and 4

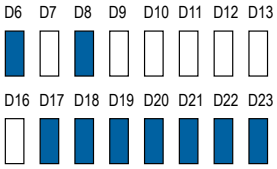
To transmit the 3G-SDI Level B video standard, follow these steps:

1. Set DIP switch[2:1] = 10
2. The demonstration runs and the LEDs indicate the following conditions:
   a. LEDs D6 and D7 indicate the internal video pattern generator signal standard.
   b. LEDs D8 and D9 indicate the receive video standard.
   c. LED D16 blinks indicating the heartbeat of the receiver's recovered clock.

d. LED D17 illuminates when the receiver is frame locked.
e. LED D18 illuminates when the receiver is TRS locked.
f. LED D19 illuminates when the receiver is alignment locked.
g. LEDs D23, D22, D21 and D20 illuminate when the data packet of audio groups 1, 2, 3 and 4 are detected in the incoming SDI stream.

This figure shows the condition of the LEDs.

Figure 6-5: Condition of LEDs for Transmitting 3G-SDI Level B Video Standard



Additional Information 7

2014.06.30

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Additional information about the document and Altera.

Document Revision History

Date	Version	Changes
June 2014	2014.06.30	• Created a separate user guide for SDI Audio IP cores. • Removed the SDI Audio IP section from the SDI MegaCore function User Guide. • Added new registers for SDI Audio Embed IP core: SD EDP Control, Strip Control, and Strip Status. • Added new signals for SDI Audio Embed IP core: `extended_control`, `strip_control`, and `strip_control`. • Added a new register for SDI Audio Extract IP core: SD EDP Presence. • Added a new signal for SDI Audio Extract IP core: `sd_edp_presence`

How to Contact Altera

Table 7-1: Altera Contact Information

Contact[1]		Contact Method	Address
Technical support		Website	www.altera.com/support
Technical training		Website	www.altera.com/training
		Email	custrain@altera.com
Product literature		Website	www.altera.com/literature
Nontechnical support	General	Email	nacomp@altera.com
	Software licensing	Email	apgcs@altera.com

(1) You can also contact your local Altera sales office or sales representative.

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